



4X Faster Timing Closure on High-Speed Interfaces with Allegro TimingVision Environment

Cavium and Cadence

The Company

Cavium develops highly integrated semiconductor processors for intelligent networking, communications, storage, video, and security applications. Based in San Jose, California, the company also has design teams in Massachusetts, India, Taiwan, and China.

Bill Munroe is a principal PCB designer at Cavium, where he and a colleague on the Post-Silicon Validation team design evaluation boards used to confirm the correct operation and electrical characteristics of the company's network processors. The pair works on multi-layer boards for high-speed SerDes designs, typically with layer counts similar to those found in system server boards, averaging 12,000 unrouted connections and 3,000 nets.

Key Challenges

Board routing had been a time-consuming, manual process—especially as chips increasingly use standards-based high-speed interfaces (such as DDRx, PCI Express®, etc.), have increasingly sensitive signals, and have more complex electrical and layout implementation constraints.

Munroe and his colleague were using Allegro PCB Router for miscellaneous logic (and continue to do so today). But they were routing critical high-speed signals by hand, which typically took 8 to 12 weeks to lay out from start to finish, without using additional human resources. Meantime, schedule pressures were increasing as the volume of chips requiring evaluation boards grew.

“As we’re doing our board design, we’re doing our chip pin-outs. Not only are we routing our boards once, we’re selling our processors to customers who will be routing these boards over and over again,” explained Munroe. “We want to give our customers the best processor pin-out we can, make sure that our chip works very well, and ensure that our customers have ease of use as far as routability.”

It’s critical for the PCB design team to have their boards ready when the chip comes back from the fab. “As we grow the number of network processors we offer, the number of designs that we do increases. So we needed to look at where we could save time,” said Munroe.

The Solution and Results

The Cavium team didn’t have to look far for a solution, as Munroe explained: “We’re a Cadence shop.” The team implemented the Allegro TimingVision environment, available within the Allegro PCB Designer constraint-driven PCB design environment (High-Speed Option). The team also uses Allegro Constraint Manager for design constraint management.

Challenges

- Address increasing schedule pressures for complex, high-speed evaluation boards
- Accelerate timing closure process while maintaining high quality of boards
- Take on more projects with current staffing level

Cadence Solution

- Allegro® TimingVision™ environment
- Allegro PCB Designer
- Allegro PCB Router (previously known as SPECCTRA®)

Lessons Learned

- Route DDR4 signals spaced at 5X the line width for better noise/coupling immunity
- Ensure that differential pairs (static and dynamic phases) are all matched before trying to match lengths for all signals in a byte lane
- Use application modes within Allegro PCB Designer to further increase tuning efficiency
- Take advantage of user-redefinable, application-mode-sensitive “funkeys” to further shorten overall tuning process

Results

- 4X faster timing closure, without compromise on quality
- Ability to take on increased volume of PCB designs with existing resources
- Faster “what-if” analysis with fewer layers for boards for routing DDRx interfaces

The Allegro TimingVision environment has transformed Cavium’s PCB design process. With their manual process, Munroe and his colleague had to switch back and forth between their design canvas and Allegro Constraint Manager, and timing closure was completed iteratively. Feedback was delivered on a matched group level, so all signals had to meet timing before the group could go “green.” They had to manually calculate all interdependencies and margins between groups.

Now, Munroe and his colleague have real-time, color-coded visual feedback on timing and phase information right on their design canvas. The technology’s embedded timing engine analyzes signal interdependencies to develop smart delay and phase targets. “With Allegro TimingVision, everything is right there in front of you—this simple fact allows the routing process to be sped up dramatically, from the manual routing efforts we have seen that can take up to four weeks, down to four days,” noted Munroe. “The color overlays on the routes guide us to constraint resolution, so we don’t have to rely on parsing information in Allegro Constraint Manager. We can perform faster “what-if” analysis with fewer layers for our boards for routing study designs using DDRx interfaces.”

Using the Allegro technology, Munroe routed four DDR3 channels on one evaluation board in less than four days. Done manually, this would have taken four weeks. In another case, a customer was unsure whether the team could complete routing on four signal layers on a two-channel DDR design within the targeted timeframe. “As an example of what is possible with this tool, we did it in two days. Manually, this would have taken two weeks,” said Munroe.

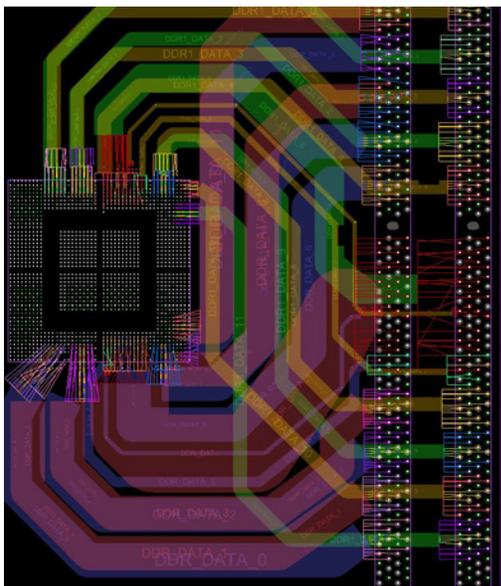


Figure 1: Initial bundling and planning stages for two-channel customer-defined placement. Allegro tools were used to generate and order the interconnect bits to be routed within each bundle.

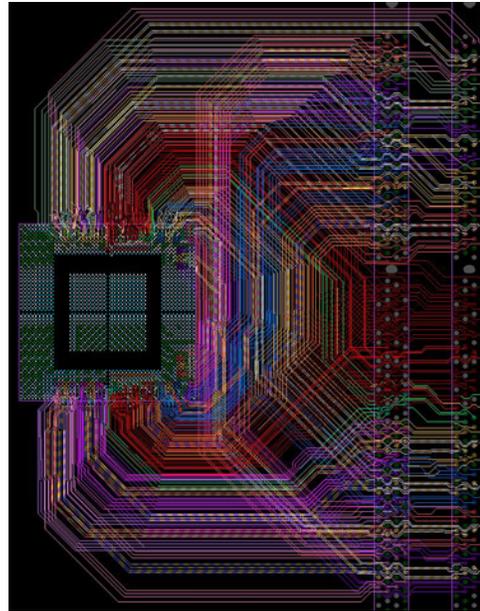


Figure 2: Cadence’s auto-interactive routing tools helped to successfully route this design with four internal signal layers.

The Cavium PCB designers also take advantage of some auto-interactive technologies while using the Allegro TimingVision environment. Auto-interactive Delay Tuning (AiDT) technology adjusts timing of the signals to meet constraints. “As an example, I can select one 12-signal DDR data byte, and use match group selection mode to tell me what the target length is. I can then adjust the match target length with AiDT, and add lengths as needed to get the line to meet the target,” Munroe explained.

The designers use Auto-interactive Breakout Technology (AiBT) with Auto-interactive Trunk Routing (AiTR) to determine whether pin-outs as proposed by the silicon package group will require more layers to break out and route to the network processor. These tools help to quickly propose new pin-outs—an advantage particularly for complex interfaces such as DDRx.

With the Allegro technologies, Munroe and his colleague can handle a larger volume of board designs—without having to spend all night in the office. “Designers don’t need to sit here hour after hour and bang their head to get something done. With the high-quality Allegro tools available, we can deliver high-quality work with greater efficiency than in the past,” he said.

Lessons Learned

As Cavium has enhanced its PCB design process, Munroe notes that when routing DDR4 designs, it’s best to route signals spaced at 5X the line width for better noise/coupling immunity. “I get a true serpentine and all of the lengths I’m looking for. My rule of thumb: if the space is available, use it,” he said.

Another tip Munroe provides is to ensure that differential pairs (static and dynamic phases) are all matched prior to matching lengths for all of the signals in a byte lane. In addition, he and his colleague perform auto-routing up front to determine the board layer count.

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Bill Munroe
Principal PCB Designer, Cavium

Also, Munroe found he could further increase tuning efficiency using the application modes within Allegro PCB Designer. He noted, “With their context-sensitive features, I have quick access to the many features available to complete the overall tuning process, including bundling/planning on these highly constrained networks. Additionally, I use application mode-sensitive “funckey”, which are user redefinable, to further shorten the overall tuning process.”

Summary

As long-time users, Cavium’s PCB designers are pleased with their bundle of Allegro PCB design tools, and will continue to learn about new solutions as they become available. “We’re a high-quality shop—that’s proven in the fact that a lot of our stuff is complete in one pass at the design, logic, and layout levels,” said Munroe. “Where Allegro TimingVision comes into play, it’s aptly named, the word vision, because that’s what it gives you.”



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